AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (canceled).

2. (currently amended): An amplifier comprising:

a gain expansion characteristic which presents an increase in gain in response to an increase in input power or output power in a certain range of the input power or the output power, and

a mechanism which compresses a larger ~~for compressing a large~~ instantaneous value, with respect to a smaller instantaneous value, of an amplitude ~~is~~ provided ~~at~~ as an input to ~~of~~ said amplifier.

3. (previously presented): An amplifier comprising:

a gain expansion characteristic which presents an increase in gain in response to an increase in input power or output power in a certain range of the input power or the output power, and

an emitter grounded amplifier circuit comprising a first bipolar transistor has a base terminal to which an input matching circuit and a cathode of a first diode for supplying a bias voltage are connected through a first impedance element which does not block a direct current,

and said first diode has an anode which is connected to a reference power supply which presents a sufficiently low impedance at high frequencies.

4. (previously presented): The amplifier according to claim 3, wherein:

said first diode has a cathode area which is 1/10 or more the size of an emitter area of said first bipolar transistor.

5. (previously presented): An amplifier comprising:

a gain expansion characteristic which presents an increase in gain in response to an increase in input power or output power in a certain range of the input power or the output power, and

a first diode is arranged in a forward direction between a base terminal of an emitter grounded amplifier circuit comprising a first bipolar transistor and a reference voltage terminal for supplying a base bias voltage to the base terminal, and a circuit comprising a second diode connected in series with a first impedance element which does not block a direct current is connected in parallel with said first diode such that said second diode is oriented in the forward direction.

6. (previously presented): The amplifier according to claim 5, wherein:

said second diode comprises a base-emitter of a third bipolar transistor which has a collector connected to a bias power supply, an emitter connected to said first impedance element, and a base connected to the reference voltage terminal.

7-20. (canceled).

21. (previously presented): The amplifier according to any of claims 3 to 6, wherein:

said first diode comprises a base-emitter of a second bipolar transistor which has a collector connected to the bias power supply, an emitter connected to said first impedance element, and a base connected to the reference voltage terminal.

22. (previously presented): The amplifier according to any of claims 3 to 6, wherein:

said first impedance element comprises a circuit which is comprised of a capacitance and a resistor in parallel.

23. (previously presented): The amplifier according to any of claims 3 to 6, wherein:

a high-frequency impedance, when said emitter grounded amplifier circuit is viewed from an input terminal, is higher than a high-frequency impedance, when a bias supply circuit is viewed from the input terminal.

24. (previously presented): A multi-stage amplifier comprising:

at least two or more amplification stages and having a gain expansion characteristic which presents an increase in gain in response to an increase in input power or output power in a certain range of the input power or the output power, and

in a power range in which the gain expansion characteristic is provided, at least one stage of said amplification stages other than a final stage has an output characteristic such that when said amplifier is applied with two wave signals at close frequencies, a phase of a third-order inter-modulation distortion rotates 90 degrees or more from the phase of the two wave signals at a time when the two wave signals match in phase.

25. (currently amended): A multi-stage amplifier comprising:

at least two or more amplification stages which have a gain extension characteristic which presents an increase in gain in response to an increase in input power or output power in a certain range of the input power or the output power, and

a mechanism which compresses a larger ~~for compressing a large~~ instantaneous value, with respect to a smaller instantaneous value, of an amplitude ~~is~~ provided as ~~at~~ an input to ~~of~~ said at least one stage ~~of said amplification stages other than a final stage~~.

26. (previously presented): A multi-stage amplifier comprising :

at least two or more amplification stages which have a gain expansion characteristic which presents an increase in gain in response to an increase in input power or output power in a certain range of the input power or the output power, and

an amplifier of at least one stage of said amplification stages other than a final stage comprises an emitter grounded amplifier circuit including a first bipolar transistor which has a base terminal connected to an input matching circuit and to a cathode of a first diode for supplying a bias, wherein said first diode has an anode connected to a reference power supply which presents a sufficiently low impedance at high frequencies.

27. (previously presented): The multi-stage amplifier according to claim 26, wherein:

said first diode has a cathode area which is 1/10 or more as large as an emitter area of said first bipolar transistor.

28. (previously presented): The multi-stage amplifier according to any of claims 26 to 27, further comprising:

a first impedance element which does not block a direct current in series with the base terminal of said emitter grounded amplifier circuit comprising the first bipolar transistor.

29. (previously presented): A multi-stage amplifier comprising:

at least two or more amplification stages which have a gain expansion characteristic which presents an increase in gain in response to an increase in input power or output power in a certain range of the input power or the output power, and

an amplifier of at least one stage of said amplification stages other than a final stage comprises a first diode arranged in a forward direction between a base terminal of an emitter grounded amplifier circuit comprising a first bipolar transistor and a reference voltage terminal for supplying a base bias voltage to the base terminal, and a circuit having a second diode connected in series with a first impedance element, connected in parallel with said first diode such that said second diode is oriented in the forward direction.

30. (previously presented): The multi-stage amplifier according to claim 29, wherein:

said second diode comprises a base-emitter of a third bipolar transistor which has a collector connected to a bias power supply, an emitter connected to said first impedance element, and a base connected to the reference voltage terminal.

31. (previously presented): The multi-stage amplifier according any of claims 26, 27, 29 and 30, wherein:

said first impedance element comprises a circuit which is comprised of a capacitance and a resistor in parallel.

32. (previously presented): The multi-stage amplifier according to any of claims 26, 27, 29 and 30, wherein:

said first diode comprises a base-emitter of a second bipolar transistor which has a collector connected to the bias power supply, an emitter connected to said first impedance element, and a base connected to the reference voltage terminal.

33. (previously presented): The multi-stage amplifier according to any of claims 26, 27, 29 and 30, wherein:

said amplifier circuit, at the input of which the mechanism for compressing the amplitude is provided, is an amplifier circuit which presents an impedance, when said emitter grounded amplifier circuit is viewed from an input terminal, that is higher than an impedance, when a bias supply circuit is viewed from the input terminal.

34. (previously presented): The multi-stage amplifier according to any of claims 26, 27, 29 and 30, wherein:

an amplification stage after said amplifier circuit having the mechanism for compressing the amplitude at the input is provided presents an impedance, when said emitter grounded amplifier circuit is viewed from an input terminal, that is higher than an impedance, when a bias supply circuit is viewed from the input terminal.